查询SA702D供应商

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

DESCRIPTION

The SA702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.7V and is compatible with the CMOS UMA1005 synthesizer from Philips and other logic circuits. The low supply current allows application in battery operated low-power equipment. Maximum input signal frequency is 1.1GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the QUBiC process. The circuit will be available in an 8-pin SO package with 150 mil package width and in 8-pin dual in-line plastic package.

FEATURES

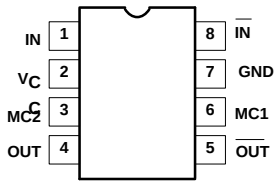
- Low voltage operation
- Low current consumption
- Operation up to 1.1GHz
- ESD hardened

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION

N, D Package



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA702N	0404B
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA702D	0174C

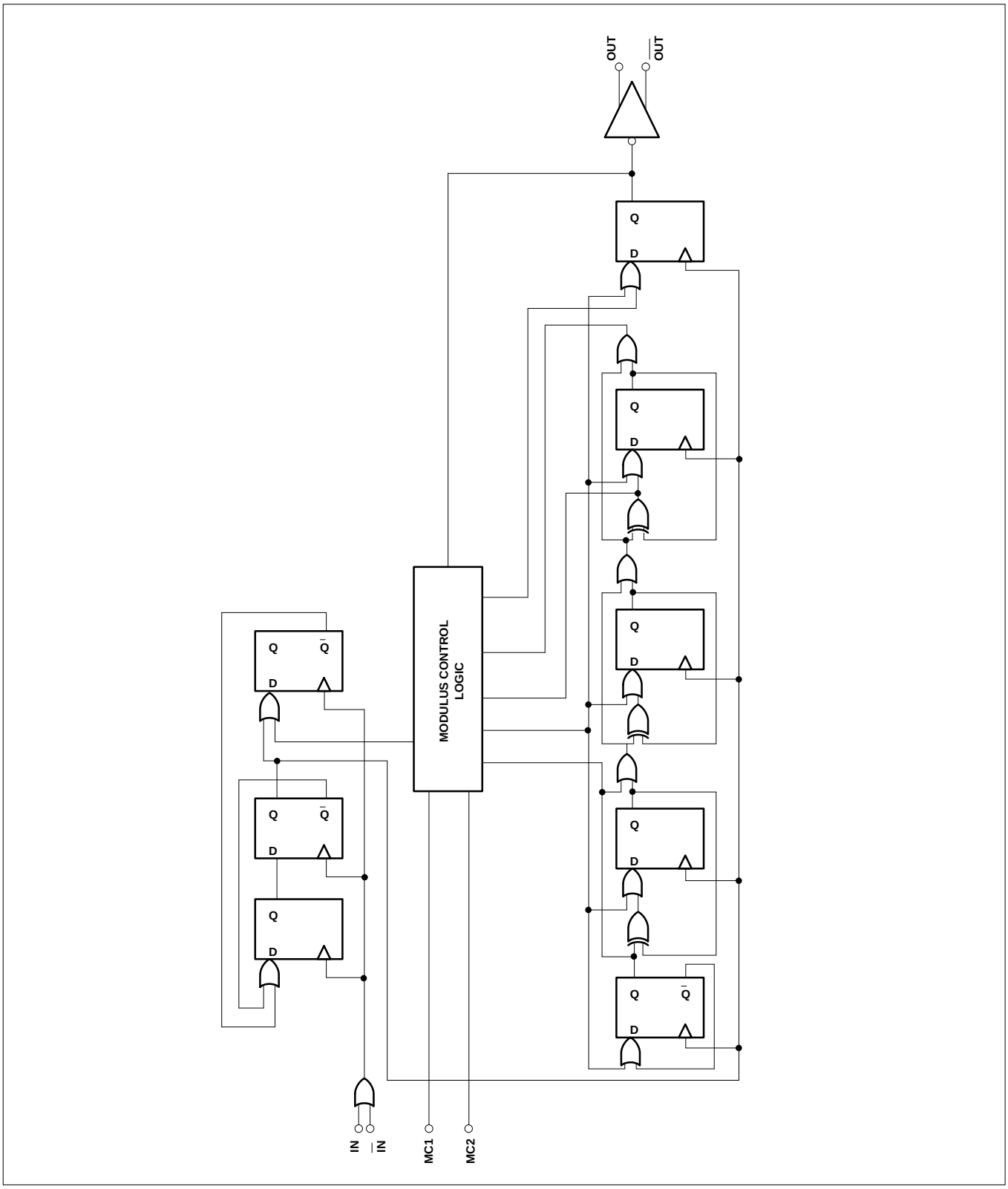
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +7.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to (V_{CC} + 0.3)	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance D package N package	158 108	°C/W

Divide by: 64/65/72 triple modulus low power ECL prescaler

SA702

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $T_A = 25^{\circ}C$ and $V_{CC} = 3.0V$; unless otherwise stated. Test circuit Figure 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range	f_{IN} = 1GHz, input level = 0dBm	2.7		6.0	V
I_{CC}	Supply current	No load		4.5		mA
V_{OH}	Output high level	I_{OUT} = 1.2mA	V_{CC}-1.4			V
V_{OL}	Output low level			V_{CC}-2.6		V
V_{IH}	MC1 input high threshold		2.0		V_{CC}	V
V_{IL}	MC1 input low threshold		–0.3		0.8	V
V_{IH}	MC2 input high threshold		2.0		V_{CC}	V
V_{IL}	MC2 input low threshold		–0.3		0.8	V
I_{IH}	MC1 input high current	$V_{MC1} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC1 input low current	$V_{MC1} = 0V$, $V_{CC} = 6V$	–100	–30		µA
I_{IH}	MC2 input high current	$V_{MC2} = V_{CC} = 6V$		0.1	50	µA
I_{IL}	MC2 input low current	$V_{MC2} = 0V$, $V_{CC} = 6V$	–100	–30		µA

AC ELECTRICAL CHARACTERISTICS

These AC specifications are valid for f_{IN} = 1GHz, input level = 0dBm, $V_{CC} = 3.0V$ and $T_A = 25^{\circ}C$; unless otherwise stated. Test circuit Fig. 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude[1]	1000pF input coupling	0.05		2.0	V_{P-P}
f_{IN}	Input signal frequency	Direct coupled input[2]	0		1.1	GHz
		1000pF input coupling			1.1	GHz
R_{ID}	Differential input resistance	DC measurement		5		kΩ
V_O	Output voltage	$V_{CC} = 5.0V$		1.6		V_{P-P}
		$V_{CC} = 3.0V$		1.2		V_{P-P}
t_S	Modulus set-up time[1]				5	ns
t_H	Modulus hold time[1]				0	ns
t_{PD}	Propagation time			10		ns

NOTES:
1. Maximum limit is not tested, however, it is guaranteed by design and characterization.
2. For f_{IN} < 50MHz, minimum input slew rate of 32V/µs is required.

DESCRIPTION OF OPERATION

The SA702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 singal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table 1.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

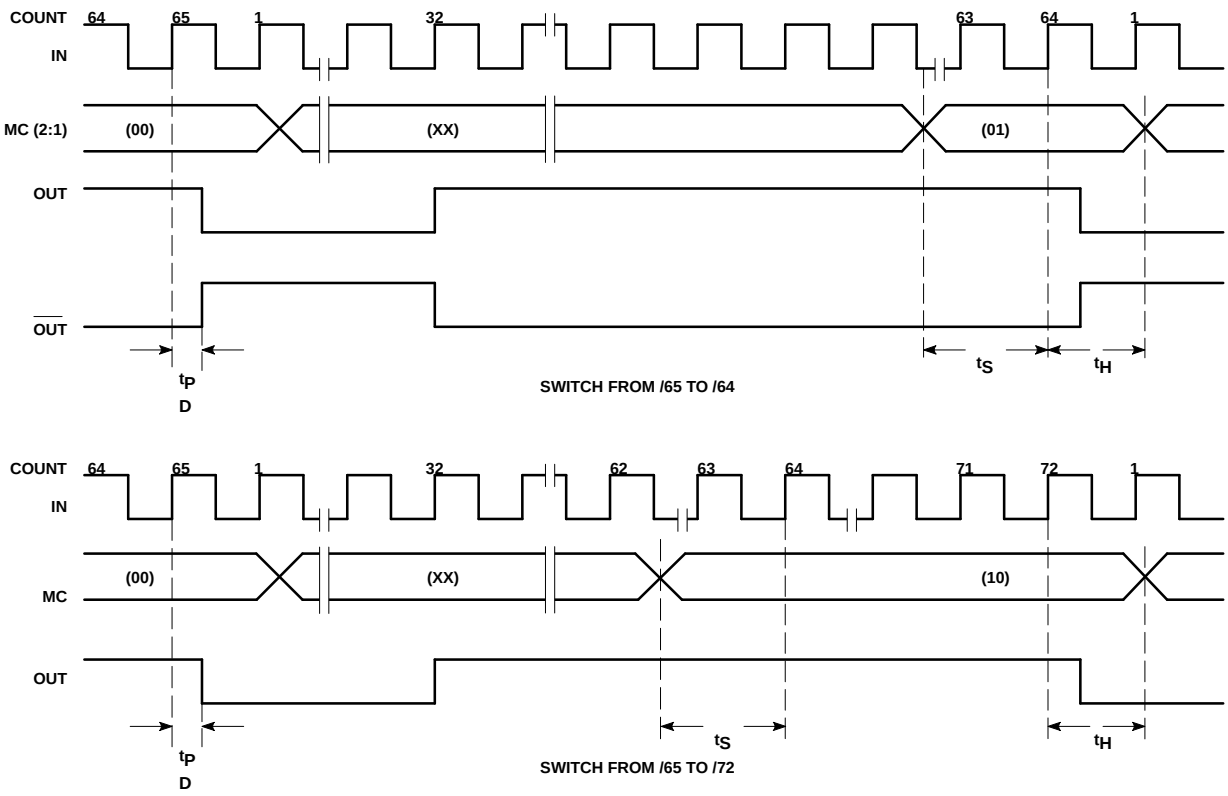
For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD}.

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

AC TIMING CHARACTERISTICS



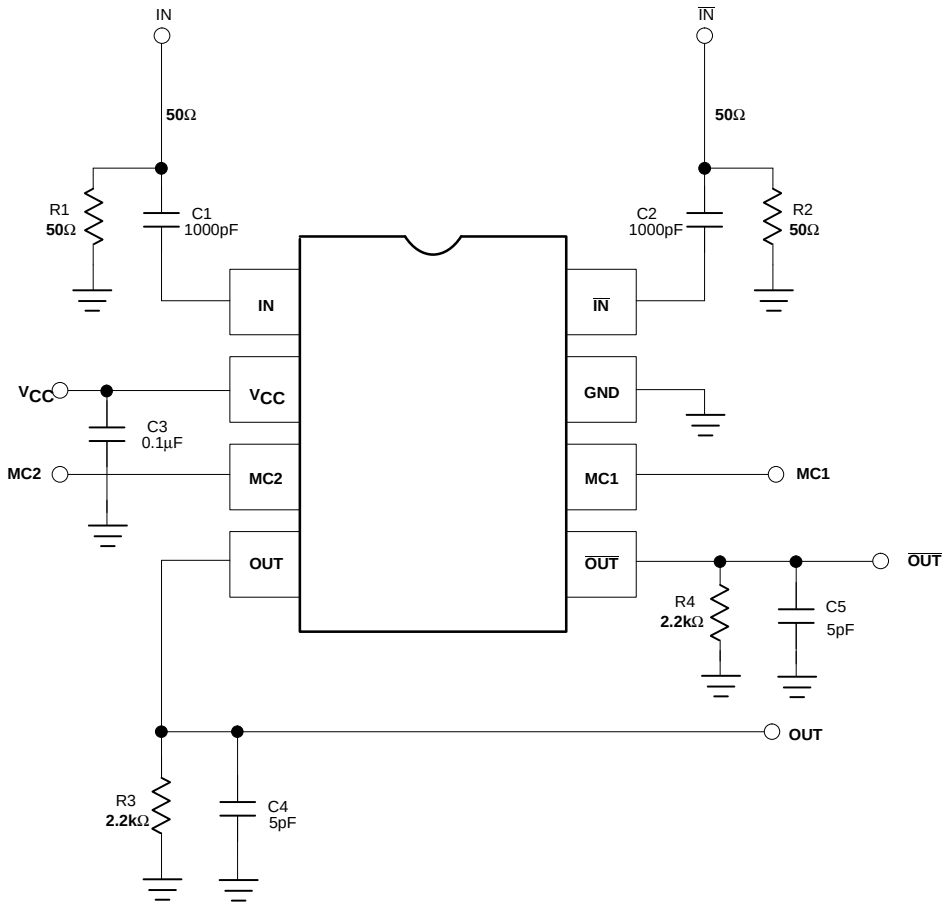


Figure 1. SA702 Test Circuit

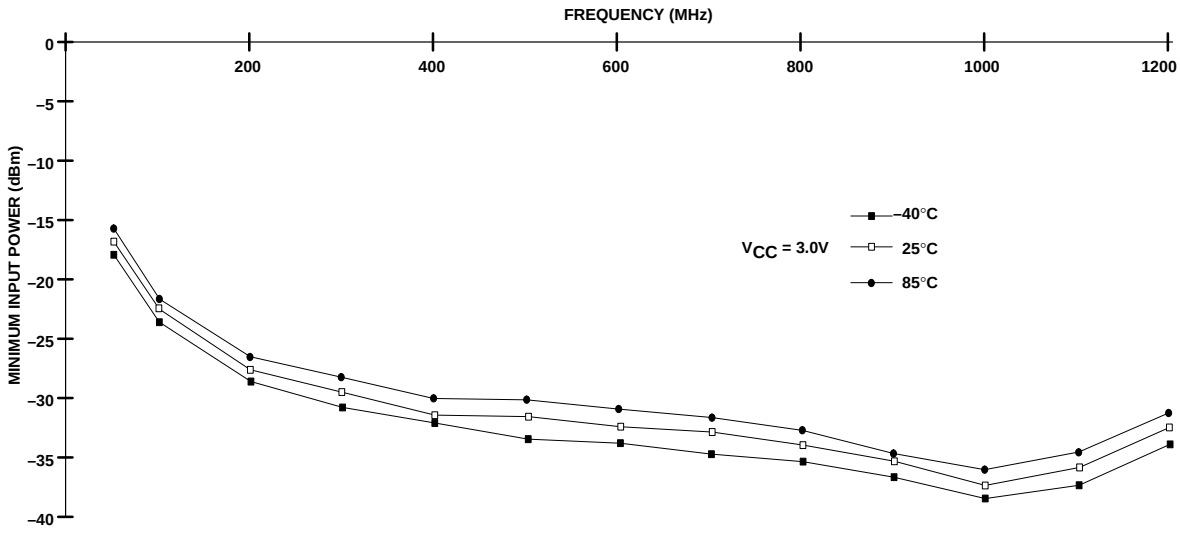


Figure 2. Minimum Input Power vs Frequency and Temperature

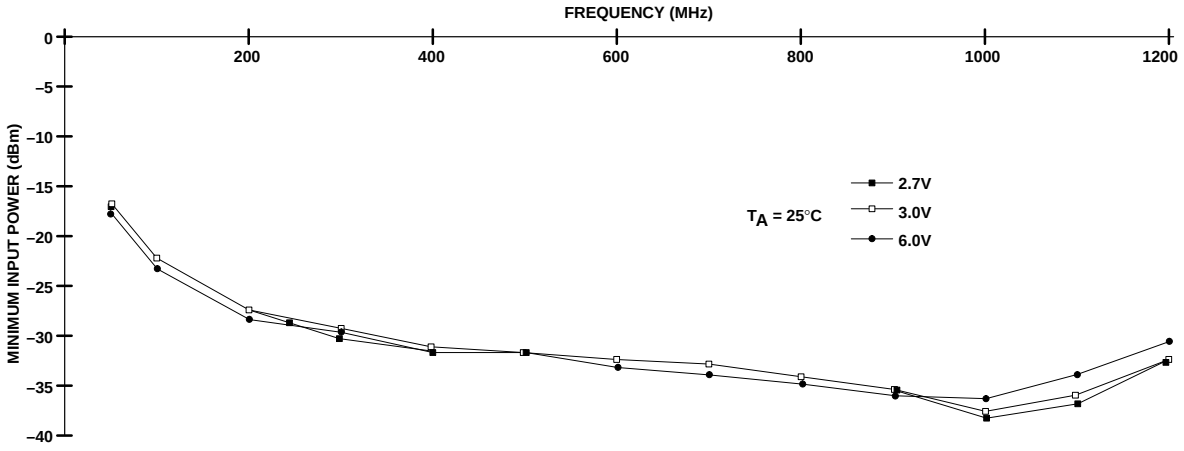


Figure 3. Minimum Input Power vs Frequency and V_{CC}

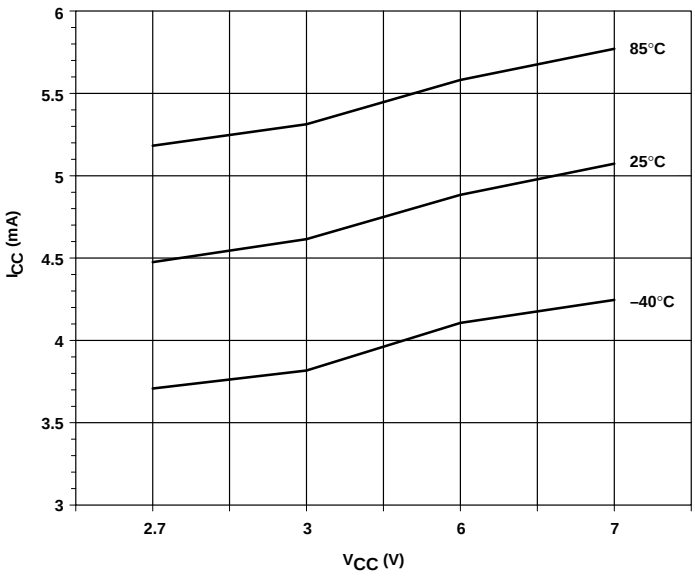
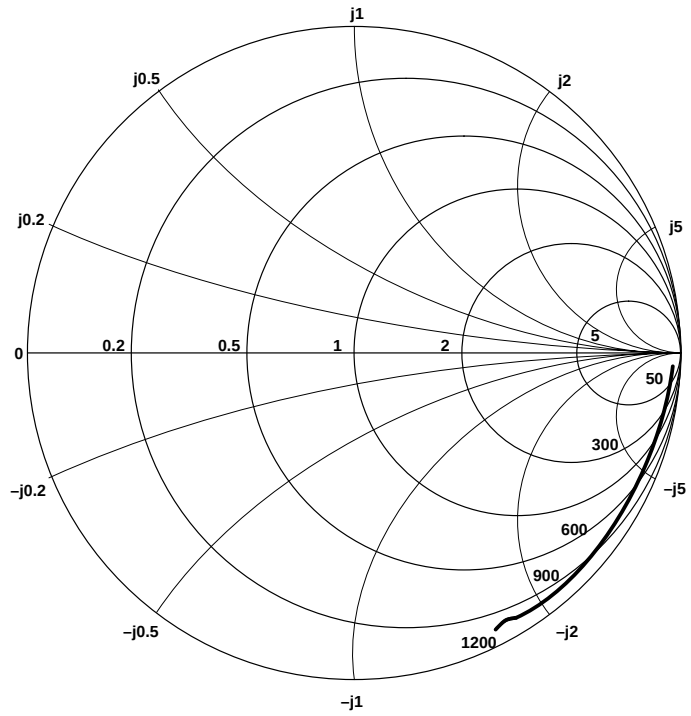


Figure 4. Supply Current vs Supply Voltage and Temperature With No Load



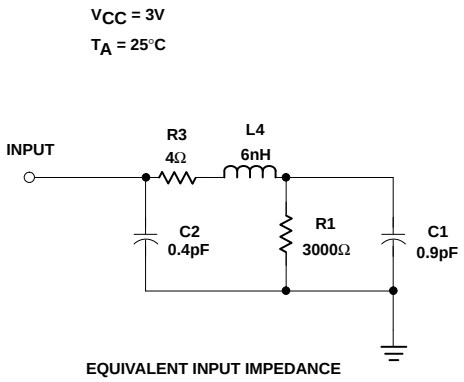
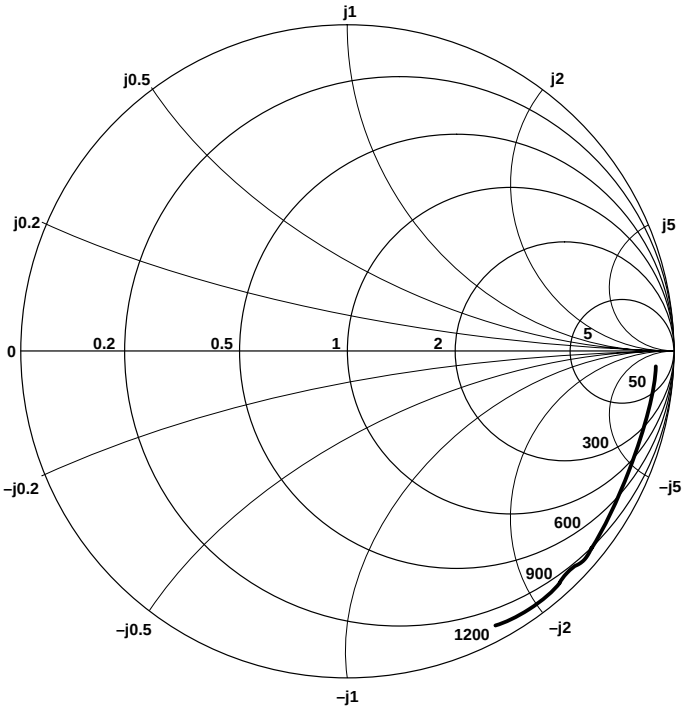


Figure 5. Typical N Package Input Impedance



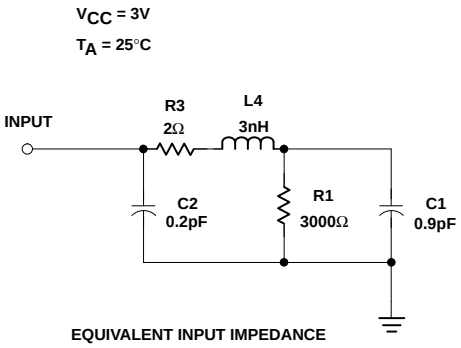


Figure 6. Typical D Package Input Impedance